

Year	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

1. A circuit arrangement comprising:  
a complementary pass transistor logic;  
a static driver connected to the  
complementary pass transistor logic and driving  
complementary input nodes to each other of the  
complementary pass transistor logic by a low swing  
voltage; and

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#### 4. A low swing charge recycling circuit

arrangement comprising:

5 a complementary pass gate stage having driving inputs to receive each of driving input signals, having complementary outputs to produce an output signal on one hand and a complementary output signal on the other and determining a logic operation of the circuit arrangement;

10 a static low swing driver stage having a signal input to receive an input signal, having a clock input to receive a clock signal, and having complementary outputs to produce low swing complementary signals to each output to be provided to the driving inputs of the complementary pass gate when the clock signal is in one of two states; and

15 an equalization stage being connected to the complementary outputs, having a clock input to receive the clock signal and producing complementary signals to the driving inputs of the complementary pass gate stage when the clock signal is in the other state, whereby  
20 a charge shared signal of an intermediate voltage level between those of the complementary outputs is shared between the driving inputs.

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5. An adder comprising:

30 a carry propagating circuit for alternatively propagating low swing driven complementary carry input signals and charge sharing complementary carry input signals;

a static low swing driver circuit receiving generate signals and producing low swing driven complementary generate signals;

35 a pass gate network receiving the complementary carry input signals, the complementary generate signals and propagate signals and being

controlled by the propagate signals for producing a sum signal by applying XOR operation to the complementary carry signals with the propagate signals;

an equalization circuit adapted to be operative alternatively with the static low swing driver circuit and providing charge sharing complementary generate signals to the pass gate network; and

a latch circuit connected to the pass gate network and latching the produced sum signal.

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6. An adder module comprising:

at least one adder connected in series, each adder being provided on the basis of one bit to be added; and

a carry input signal equalization circuit receiving carry input signals and providing charge sharing complementary carry input signals to one end of the adders connected in series,

wherein the adder includes:

a carry propagating circuit for alternatively propagating low swing driven complementary carry input signals and the charge sharing complementary carry input signals;

a static low swing driver circuit receiving generate signals and producing low swing driven complementary generate signals;

a pass gate network receiving the complementary carry input signals, the complementary generate signals and propagate signals and being controlled by the propagate signals for producing a sum signal by applying XOR operation to the complementary carry signals with the propagate signals;

an equalization circuit adapted to be operative alternatively with the static low swing driver

circuit and providing charge sharing complementary generate signals to the pass gate network; and  
a latch circuit connected to the pass gate network and latching the produced sum signal.

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7. The adder module as claimed in claim 6  
10 further comprising:  
a carry propagating path for propagating the complementary carry input signals in series of bits;  
a carry skip path bypassing the adders connected in series in order to pass the complementary  
15 carry input signals transparently; and  
a carry conflict-free circuit for protecting a conflict of the propagated carry input signals and the passed carry input signals.

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